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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,310	11/25/2003	Go Iwasaki	81788.0261	7084
26021 7590 02/02/2007 HOGAN & HARTSON L.L.P. 1999 AVENUE OF THE STARS SUITE 1400 LOS ANGELES, CA 90067			EXAMINER LE, THONG QUOC	
			ART UNIT 2827	PAPER NUMBER
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		02/02/2007	PAPER	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<p align="center"><b>Office Action Summary</b></p>	<p>Application No.</p> <p align="center">10/721,310</p>	<p>Applicant(s)</p> <p align="center">IWASAKI, GO</p>	
	<p>Examiner</p> <p align="center">Thong Q. Le</p>	<p>Art Unit</p> <p align="center">2827</p>	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 November 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 and 15-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-2,8,15-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| <p>1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)</p> <p>2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)</p> <p>3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br/> Paper No(s)/Mail Date <u>09/11/2006</u></p> | <p>4) <input type="checkbox"/> Interview Summary (PTO-413)<br/> Paper No(s)/Mail Date. _____</p> <p>5) <input type="checkbox"/> Notice of Informal Patent Application</p> <p>6) <input type="checkbox"/> Other: _____</p> |
|---|---|

### DETAILED ACTION

1. Amendment filed on 11/22/2006 has been entered.
2. Claims 1-10, 15-19 are presented for examination.

### *Information Disclosure Statement*

3. The information disclosure statement filed 09/11/2006 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.
4. Information disclosed and list on PTO 1449 was not considered, because no copy of foreign patent document submitted.

### *Response to Arguments*

5. Applicant's arguments filed 11/22/2006 have been fully considered but they are not persuasive.

Applicant argued that the claims contain a **plurality of resistors** is improper.

The Office Action states that the Kurisu publication discloses the presence of plural resistors formed between the output buffer circuit and output terminal. More specifically, the Office Action states that Figure 6 of the publication shows a single resistor L between common node TOUT and output TRV. The referenced single resistor L does not meet the limitation of claim 1, which requires plural resistors, and the single referenced resistor L of Figure 6 further does not meet the positional limitation of claim 1 that requires resistors between the unit circuits' common nodes and the common connecting point for the buffer. In the Figure 6 of

In all claims, applicant discloses the first resistors formed between a common nodes of plurality of unit circuits and the common connecting point as shown in Figure 1 of present invention and Figures 1, 14-15 are embodiments of present invention, which is described in description of the preferred embodiments section. For example, in figure 1 of present invention, first resistors is R1, and common connecting point is OUT, common nodes of plurality of circuits is C11 of B1 and B2, and claimed invention is R1 located between C11 and OUT, and then it the same invention in Figure 4 of Kurisu et al.

In present invention, applicant does not provide "a plurality of resistors " limitation in written description. In reference Kurisu, Figure 6 shows first resistors L is located between common nodes of circuits B1, B20, B21 (TOUT) and common connecting point TRV. It is clearly to overcome the limitation in present claims.

This is true when the limitation " first resistors formed respective between said common nodes of the plurality of unit circuits and common connecting point" is applied for Figures 1, 7-8, 14-15, R1 used in present invention. Otherwise, the inventions of these Figures will be invalid invention.

As described above, the references Kurisu et al. (Pub. U.S. Patent No. 2002/0030517), and Kohno (U.S. 6,041,013) still stand.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 1-2,8 are rejected under 35 U.S.C. 102(e) as being anticipated by Kurisu et al. (Pub. U.S. Patent No. 2002/0030517). Regarding claims 1-2, Kurisu et al. disclose an output buffer circuit (Figure 5) comprising:

a plurality of unit circuits (Figure 5 B20) in each of which a pull-up transistor (Figure 5, P3) controlled by a first input signal (Figure 5, signal TS go through INV3) is connected between a high-potential power supply (Figure 5, VDD) and common node (Figure 5), and a first pull-down transistor (Figure 5, N2) controlled by a second input signal (Figure 5, signal from TB) and a second pull-down transistor (Figure 5, N3) controlled by a third input signal (Figure 5, signal from TS) are connected in series between said common node (Figure 5, N2 and N3 in series) and a low-potential power

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supply (Figure 5, VSS, [0014]); an output terminal (Figure 5, TRV) connected to a common connecting point (Figure 5, TOUT) of said common nodes of said plurality of unit circuits (Figure 5); and first resistors (Figure 5, L, [0062], impedance of L) formed respectively between said common nodes of said plurality of unit circuits and said common connecting point (Figure 5). (L is a resistor (a impedance is defined in [0062]), or reference U.S. 6,204,692, Nakagawa defined transmission line by means of resistors in column 10 lines 12-13. L is a impedance of resistors in transmission line from TOUT to TRV). Regarding claim 8, Kurisu et al disclose wherein each of said pull-up and pull-down transistors is a MIS transistor (Figure 5, P3, N2).

### ***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurisu et al (Pub. U.S. 2002/0030517) in view of Kohno (U.S. Patent No. 6,041,013). Regarding claims 15-16, Kurisu et al. disclose a semiconductor memory (Figure 6) comprising: a plurality of memory cells (a plurality of memory cells is seen to be inherent in the prior art memory device) ; a plurality of terminals (Figure 6, B20, B21)

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including an output terminal (Figure 6, TOUT); and said output buffer circuit (Figure 6) comprising a plurality of unit circuits (Figure 6, B20,B21) in each of which a pull-up transistor (P3) controlled by a first input signal (TS1 through INV3) is connected between a high-potential power supply (VD) and common node (Figure 6) and a pull-down transistor (Figure 6, N3) controlled by a second input signal (Figure 6, TS1) is connected between said common node and a low-potential power supply (Figure 6, VSS), and comprising first resistors (Figure 6, L, as described in claim 1) connected respectively between said common nodes of said plurality of unit circuits and a common connecting point (Figure 6, TOUT) of said common nodes, and wherein said first resistors are formed between said output buffer circuit and output terminal (Figure 6, impedance I resistor is between common node TOUT and output TRV).

Kurisu et al. as described above, fails to disclose arrangement of position of an output buffer circuit is positioned adjacent to the memory cell. However, Kohno discloses an output buffer is positioned adjacent the memory cell in Figure 2, 30-B1-30B8 or in Figure 8, output buffer 32-An is adjacent to memory cell. At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to arrange the output buffer circuit in position of adjacent to memory cell. Applicant has not disclosed that output buffer circuit positioned adjacent to memory cell provides an advantage, is used for particular purpose, or solves a state problem. Therefore, it would have been obvious to a person of ordinary skill in this art to modify the location of output buffer circuit in Kohno to obtain the invention as specified in claim 15.

### **Allowable Subject Matter**

9. Claims 3-7, 9-10, 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 3-7, 9-10, 17-19 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Houghton et al. (U.S. Patent No. 5,355,029), Kurisu et al. (Pub. U.S. Patent No. 2002/0030517), Kohno (U.S. Patent No. 6,041,013), and others, does not teach the claimed invention having a second resistors are arranged as in claims 3-7, and the structure of transistors and resistor as claims 9-10 disclosed, and wherein if the number of said first resistors is an even number, said first resistors are symmetrically arranged with respect to a central line of said output buffer circuit and output terminal, and have the same value, the same size, and the same shape as claim 17 disclosed, and wherein said first resistors are formed on at least not less than one of three sides of said output terminal, which do not oppose said output buffer circuit as claims 18-19 disclosed.

### **Conclusion**

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not



mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zarabian Amir can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thong Q. Le  
Primary Examiner  
Art Unit 2827

